

AMENDMENT TO THE CLAIMS

IN THE CLAIMS:

The claims are original and have not been amended. (All claims listed)

1 1. (Original) A cache-coherent device comprising:
2 a plurality of client ports, each to be coupled to one of a plurality of port components;
3 a plurality of sub-unit caches, each coupled to one of said plurality of client ports and
4 assigned to one of said plurality of port components; and
5 a coherency engine coupled to said plurality of sub-unit caches.

1 2. (Original) The device of claim 1 wherein said plurality of port components include
2 processor port components.

1 3. (Original) The device of claim 1 wherein said plurality of port components include
2 input/output components.

1 4. (Original) The device of claim 3 wherein said plurality of sub-unit caches include
2 transaction buffers using a coherency logic protocol.

1 5. (Original) The device of claim 4 wherein said coherency logic protocol includes a
2 Modified-Exclusive-Shared-Invalid (MESI) cache coherency protocol.

1 6. (Original) A processing system comprising:
2 a processor;
3 a plurality of port components; and
4 a cache-coherent device coupled to said processor and including a plurality of client
5 ports, each coupled to one of said plurality of port components, said cache-coherent device
6 further including a plurality of caches, each coupled to one of said plurality of client ports and
7 assigned to one of said plurality of port components, and a coherency engine coupled to said
8 plurality of caches.

1 7. (Original) The processing system of claim 6 wherein said plurality of port components
2 include processor port components.

1 8. (Original) The processing system of claim 6 wherein said plurality of port components
2 include input/output components.

1 9. (Original) In a cache-coherent device including a coherency engine and a plurality of
2 client ports, a method for processing a transaction, comprising:
3 receiving a transaction request at one of said plurality of client ports, said transaction
4 request includes an address; and
5 determining whether said address is present in one of a plurality of sub-unit caches, each
6 of said sub-unit caches assigned to said of a plurality of client ports.

1 10. (Original) The method of claim 9 wherein said transaction request is a read transaction
2 request.

1 11. (Original) The method of claim 10 further comprising:
2 transmitting data for said read transaction request from said one of said plurality of sub-
3 unit caches to one of said plurality of client ports.

1 12. (Original) The method of claim 11 further comprising:
2 prefetching one or more cache lines ahead of said read transaction request; and
3 updating the coherency state information in said plurality of sub-unit caches.

1 13. (Original) The method of claim 12 wherein the coherency state information includes a
2 Modified-Exclusive-Shared-Invalid (MESI) cache coherency protocol.

1 14. (Original) The method of claim 9 wherein said transaction request is a write transaction
2 request.

1 15. (Original) The method of claim 14 further comprising:
2 modifying coherency state information for a cache line in said one of said plurality of
3 sub-unit caches;
4 updating coherency state information in others of said plurality of sub-unit caches by said
5 coherency engine; and

6 transmitting data for said write transaction request from said one of said plurality of sub-
7 unit caches to memory.

a 1 16. (Original) The method of claim 15 further comprising:
2 modifying coherency state information of said write transaction request in the order
3 received; and
4 pipelining multiple write requests.

1 17. (Original) The method of claim 16 wherein the coherency state information includes a
2 Modified-Exclusive-Shared-Invalid (MESI) cache coherency protocol.